

Document Title**256Kx16 Low Voltage & Low Power SRAM Datasheets for 48-CSP****Revision History**

<u>Revision No</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	February 4, 1997	Preliminary
0.1	Revised - Change datasheet format - Remove commercial part from product - Power dissipation improved 0.7 to 1.0W - $V_{IL(MAX)}$ improved 0.4 to 0.6V. - I_{CC2} decreased 90 to 60mA. - I_{CC1} (Read/Write) change 20/40 to 10/45mA - I_{CC} Read change 20 to 10mA, and remove write value.	February 12, 1998	Preliminary
0.11	Errata correction	August 17, 1998	

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256Kx16 Low Power and Low Voltage CMOS Static RAM with 48-CSP(Chip Scale Package)

FEATURES

- Process Technology : CMOS
- Organization :256Kx16
- Power Supply Voltage
 - KM616V4000BZ Family : 3.0 ~ 3.6V
 - KM616U4000BZ Family : 2.7 ~ 3.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 48-CSP with 0.75 pitch

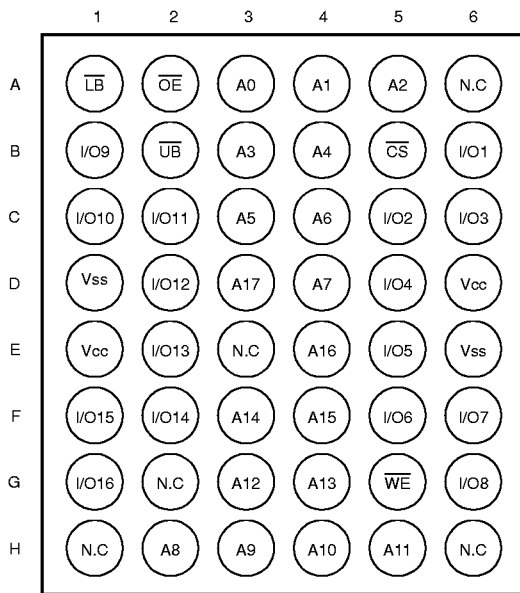
GENERAL DESCRIPTION

The KM616V4000BZ and KM616U4000BZ families are fabricated by SAMSUNG's advanced CMOS process technology. The families support industrial operating temperature ranges and have very small size with 0.75 ball pitch and 6x8 ball array. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

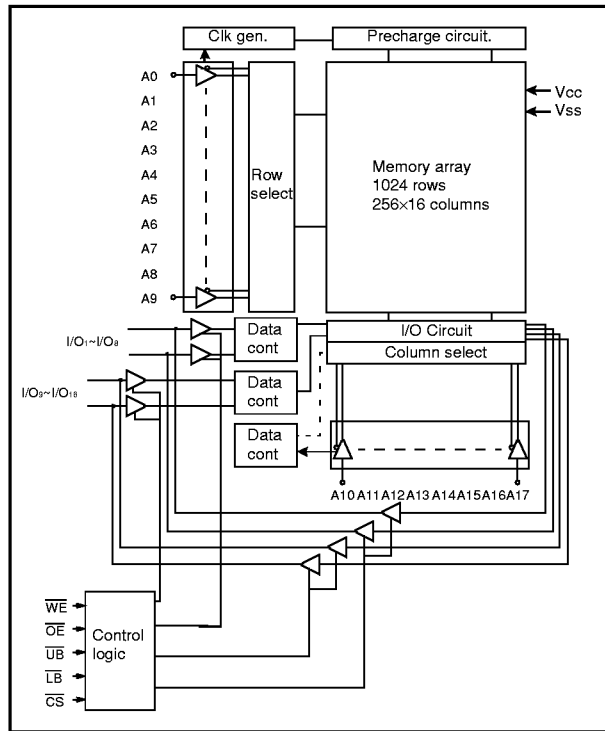
Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
KM616V4000BLZI-L	Industrial (-40~85°C)	3.0~3.6V	85	20µA	60mA	48-CSP(6x8 ball area with 0.75mm ball pitch)
KM616U4000BLZI-L		2.7~3.3V	100			

48-CSP PIN TOP VIEW



Name	Function	Name	Function
\overline{CS}	Chip Select Input	\overline{LB}	Lower Byte (I/O1~8)
\overline{OE}	Output Enable Input	\overline{UB}	Upper Byte(I/O9~16)
\overline{WE}	Write Enable Input	Vcc	Power
A0~A17	Address Inputs	Vss	Ground
I/O1~I/O16	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
KM616V4000BLZI-8L	48-CSP, 85ns, 3.3V, LL
KM616U4000BLZI-10L	48-CSP, 100ns, 3.0V, LL

FUNCTIONAL DESCRIPTION

CS	OE	WE	LB	UB	I/O1-8	I/O9-16	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
L	H	H	X ¹⁾	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	-40 to 85	°C	KM616V4000BLZI, KM616U4000BLZI
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	KM616V4000BZ Family KM616U4000BZ Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IN}	KM616V4000BZ, KM616U4000BZ Family	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	KM616V4000BZ, KM616U4000BZ Family	-0.3 ³⁾	-	0.6	V

Note:

1. Industrial Product : T_A=-40 to 85°C, otherwise specified
2. Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
3. Undershoot : -3.0V in case of pulse width ≤ 30ns
4. Overshoot and undershoot is sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled not, 100% tested

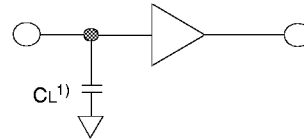
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IL} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH} , Read	-	-	10	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA $\overline{CS} \leq 0.2V$, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V	Read	-	-	10	mA
			Write	-	-	45	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}	-	-	60	mA	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.2	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$	-	-	0.5	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Others inputs = 0~V _{CC}	-	-	20	μA	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V
 Input rising and falling time : 5ns
 Input and output reference voltage : 1.5V
 Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS (KM616V4000BZ : $V_{CC}=3.0\sim 3.6\text{V}$, KM616U4000BZ : $V_{CC}=2.7\sim 3.3\text{V}$, Industrial product : $T_A=-40$ to 85°C)

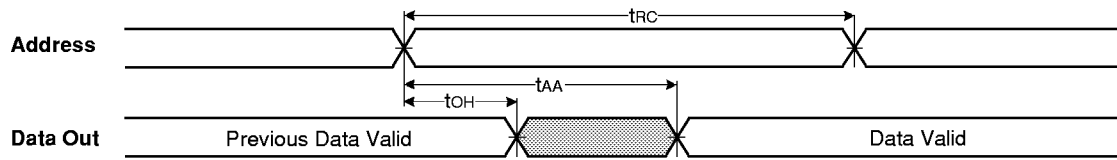
Parameter List		Symbol	Speed Bins				Units
			85ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	85	-	100	-	ns
	Address access time	t _{AA}	-	85	-	100	ns
	Chip select to output	t _{CO}	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	40	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ enable to low-Z output	t _{BLZ}	5	-	5	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ valid to data output	t _{BA}	-	40	-	50	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	30	ns
	$\overline{\text{OE}}$ disable to high-Z output	t _{OHZ}	0	25	0	30	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ disable to high-Z output	t _{BHZ}	0	25	0	30	ns
	Output hold from address change	t _{OH}	10	-	15	-	ns
Write	Write cycle time	t _{WC}	85	-	100	-	ns
	Chip select to end of write	t _{CW}	70	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	70	-	80	-	ns
	Write pulse width	t _{WP}	55	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	30	ns
	Data to write time overlap	t _{DW}	35	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ valid to end of write	t _{BW}	70	-	80	-	ns

DATA RETENTION CHARACTERISTICS

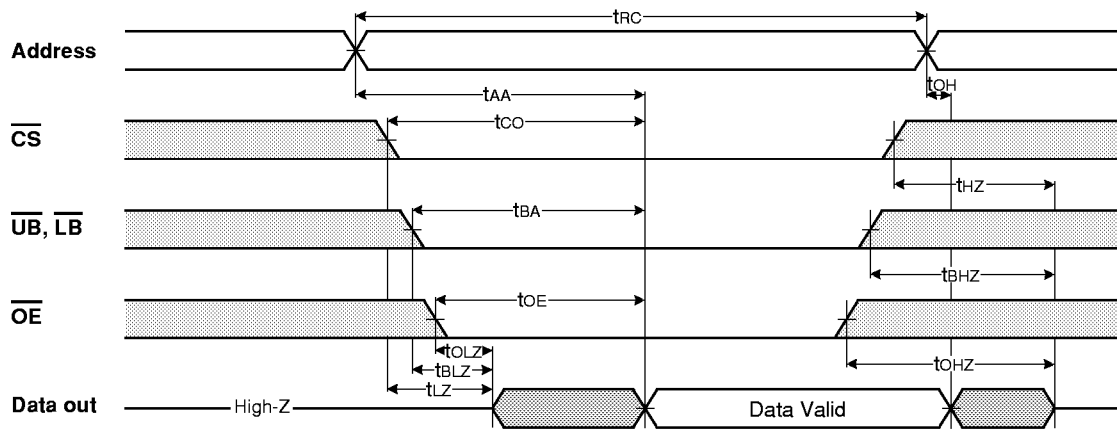
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC}=3.0\text{V}$, $\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$	-	0.5	20	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{il}$, $\overline{WE}=V_{ih}$, \overline{UB} or and $\overline{LB}=V_{il}$)



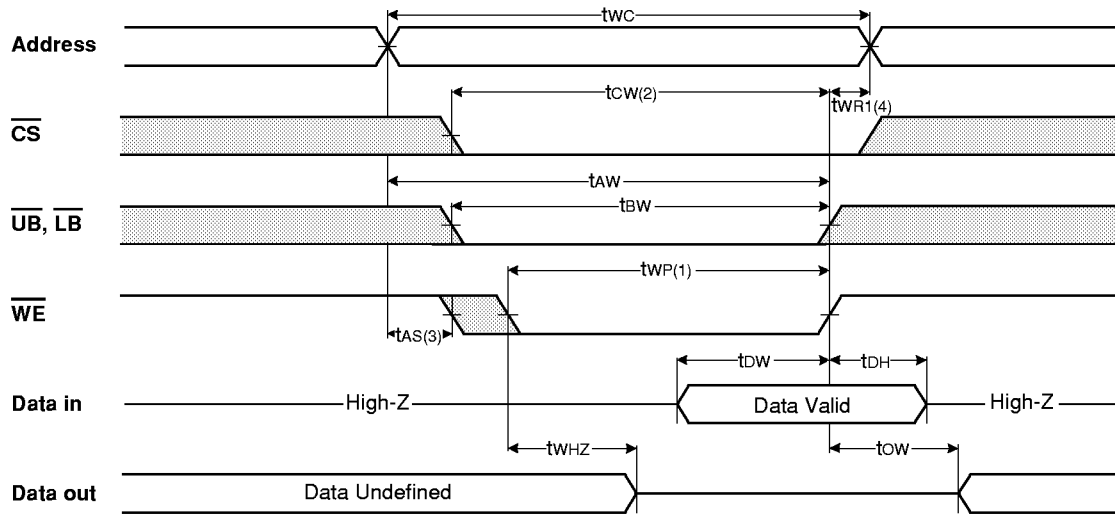
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{ih}$)



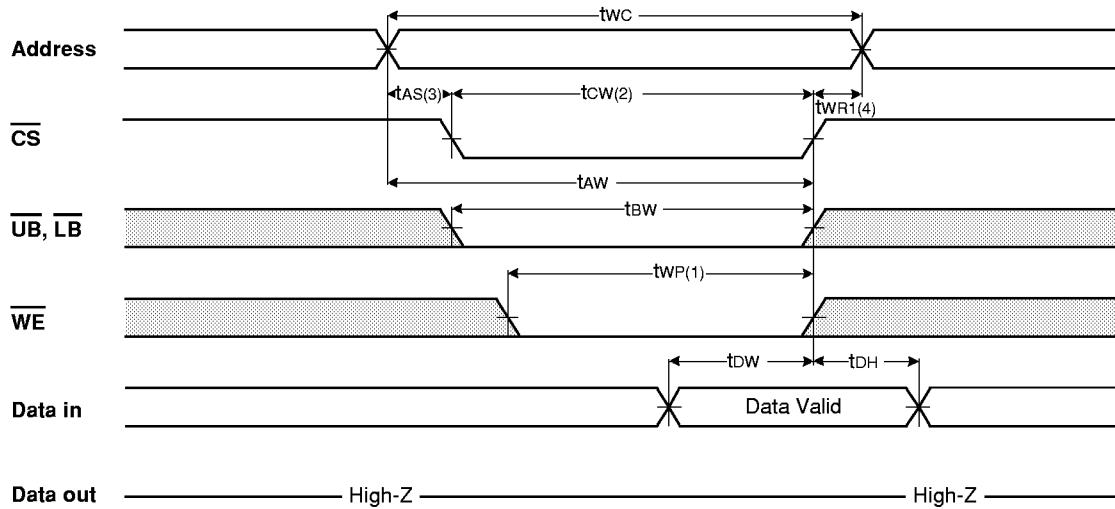
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

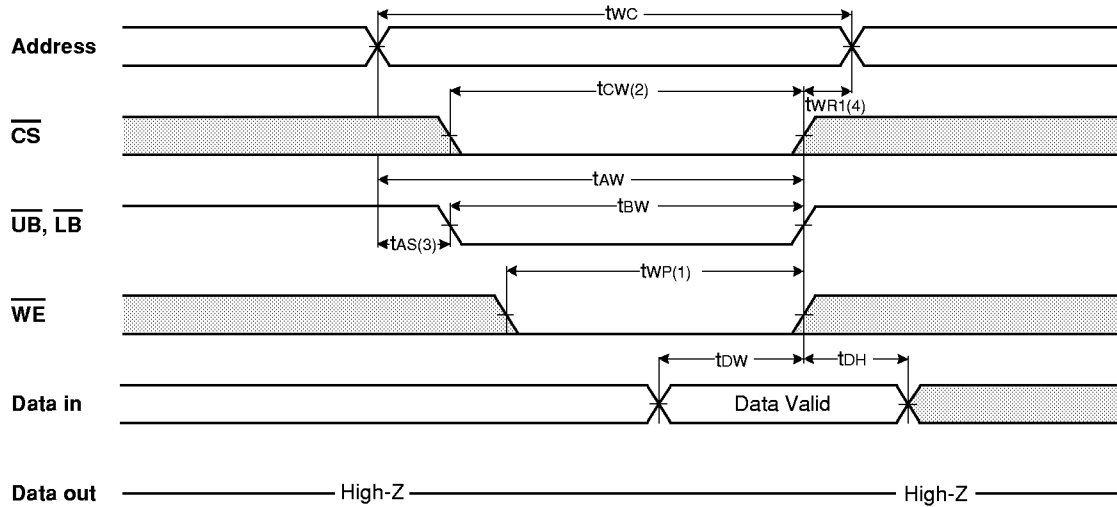
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)



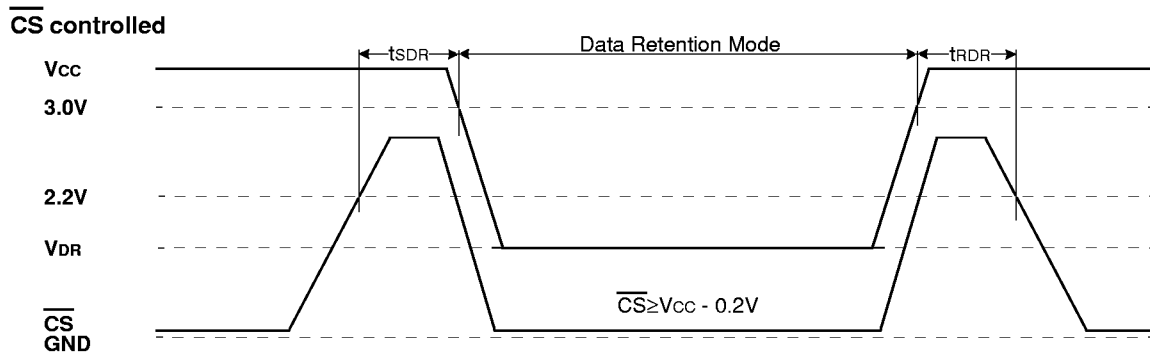
TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{UB} , \overline{LB} Controlled)



NOTES (WRITE CYCLE)

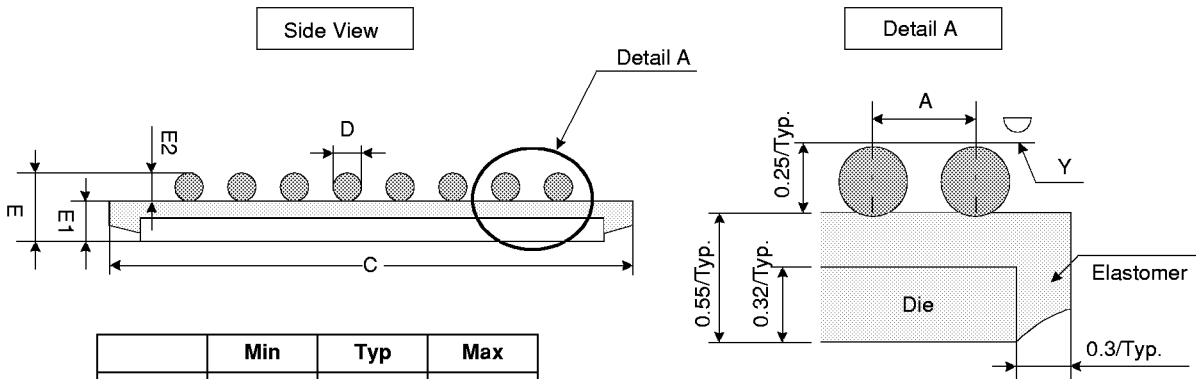
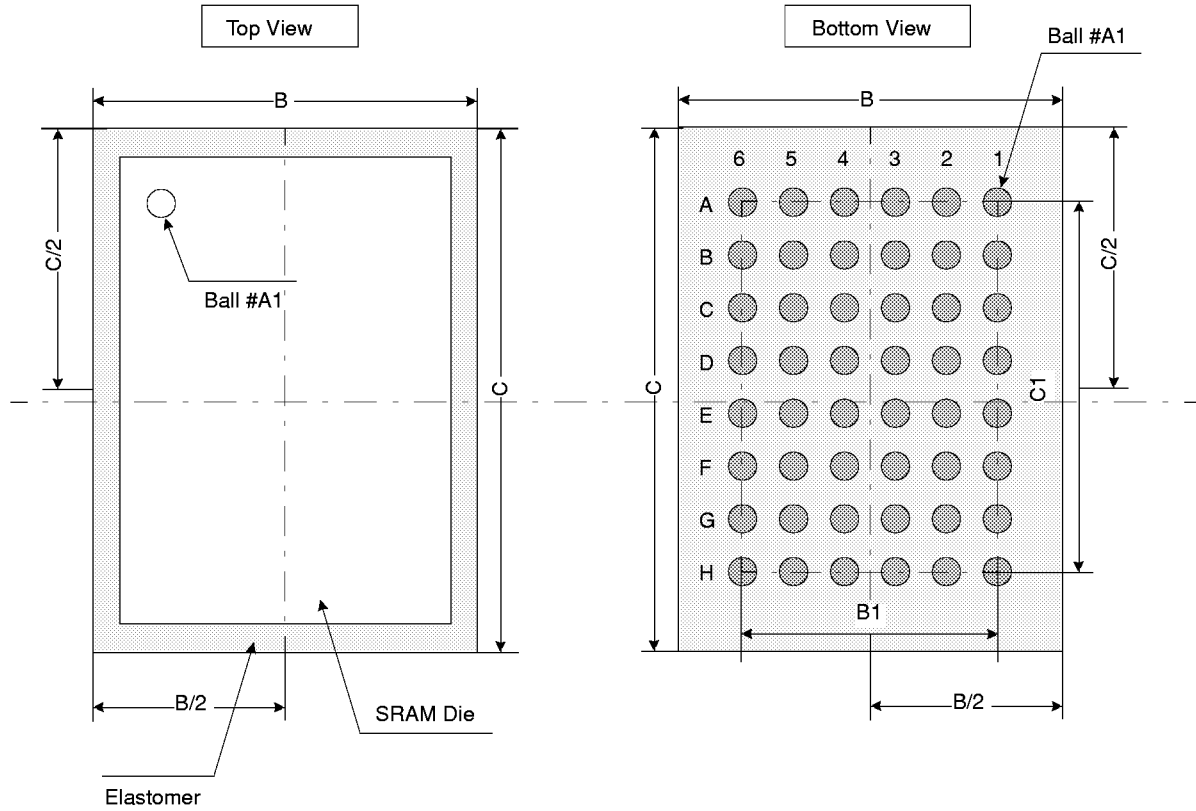
1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR1} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as \overline{CS} or \overline{WE} going high.

DATA RETENTION WAVE FORM



PACKAGE DIMENSIONS

Unit : millimeter(inch)



	Min	Typ	Max
A	-	0.75	-
B	7.10	7.20	7.30
B1	-	3.75	-
C	11.55	11.65	11.75
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08

Notes.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)